What is claimed is:

Sub A1

1. An integrated circuit structure which comprises

(a) a substrate;

(b) a layer of a first dielectric material on the substrate;

(c) a plurality of spaced apart metal contacts on the layer of the first dielectric material;

(d) a space between adjacent metal contacts, each space being filled with the first dielectric material;

(e) a recess in the filled spaces of the first dielectric material extending from a level at a top of the metal contacts a part of the distance toward the substrate;

(f) a second dielectric layer on at least some of the metal contacts and in the recesses on the filled spaces of the first dielectric material such that there is optionally a gap in at least one of the recesses of the second dielectric layer at a side wall of a metal contact;

(g) an additional layer of the first dielectric material on the second dielectric layer;

(h) at least one via extending through the additional layer of the first dielectric layer and the second dielectric layer extending to the top of at least one of the metal contacts and optionally to a gap;

wherein the first dielectric material and the second dielectric material have substantially different etch resistance properties.

2. The integrated circuit structure of claim 1 wherein the via is filled with at least one metal.

Sub A2

3. The structure of claim 1 wherein the first dielectric material is organic and the second dielectric material is inorganic.

4. The structure of claim 1 wherein the first dielectric material is inorganic and the second dielectric material is organic.

5. An integrated circuit structure which comprises

(a) a substrate;

(b) a layer of a first dielectric material on the substrate;

(c) a plurality of spaced apart metal contacts on the layer of the first dielectric material;

(d) a space between adjacent metal contacts, each space being filled with a second dielectric material;

(e) a recess in the filled spaces of the second dielectric material extending from a level at a top of the metal contacts a part of the distance toward the substrate;

(f) an additional layer of the first dielectric layer on at least some of the metal contacts and in the recesses on the filled spaces of the second dielectric material such that there is optionally a gap in at least one the recesses of the first dielectric layer at a side wall of a metal contact;

(g) at least one via extending through the additional layer of the first dielectric layer extending to the top of at least one of the metal contacts and optionally to a gaps;

wherein the first dielectric material and the second dielectric material have substantially different etch resistance properties.

6. The integrated circuit structure of claim 5 wherein the via is filled with at least one metal.

7. The structure of claim 5 wherein the first dielectric material is organic and the second dielectric material is inorganic.

8. The structure of claim 5 wherein the first dielectric material is inorganic and the second dielectric material is organic.

9. A process for producing an integrated circuit structure which comprises

(a) providing a substrate;

(b) depositing a layer of a first dielectric material onto the substrate;

(c) forming a pattern of metal contacts on the layer of the first dielectric material including a space between adjacent metal contacts;

(d) depositing a layer of the first dielectric material on a top surface of the metal contacts and filling in the space between the metal contacts with the first dielectric material;

(e) removing the first dielectric material from the top surface of the metal contacts and removing an upper portion of the first dielectric material from the filled space between the metal contacts to form a recess;

(f) depositing a layer of a second dielectric material on the metal contacts and filling the recess with second dielectric material, wherein the first dielectric material and the second dielectric material have substantially different etch resistance properties;

(g) depositing an additional layer of the first dielectric material over the layer of the second dielectric material;

(h) depositing a layer of a photoresist on the additional layer of the first dielectric material;

(i) imagewise removing a portion of the photoresist over some of the metal contacts and optionally over a portion of at least one of the filled recesses adjacent to a side wall of a metal contact;

(j) removing the portion of the layer of the additional layer of the first dielectric material under the removed portion of the photoresist;

(k) removing the balance of the photoresist layer, and removing the portion of the second dielectric material under the removed portion of the additional layer of the first dielectric material until reaching at least one of the metal contacts and optionally reaching the space filled by the first dielectric material thus forming at least one via through the additional layer of the first dielectric material and through the layer of the second dielectric material.

10. The process of claim 9 further comprising:

(n) depositing a layer of a barrier metal on the additional layer of the first dielectric material, and on inside walls and a floor of the at least one via;

(o) filling the at least one via with a fill metal and depositing a layer of a fill metal on the layer of the barrier metal;

(p) removing the fill metal layer, the barrier metal layer and optionally the additional layer of the first dielectric material.

11. The process of claim 9 wherein the first dielectric material is organic and the second dielectric material is inorganic.

12. The process of claim 9 wherein the first dielectric material is inorganic and the second dielectric material is organic.

13. A process for producing an integrated circuit structure which comprises

(a) providing a substrate;

(b) depositing a layer of a first dielectric material onto the substrate;

(c) forming a pattern of metal contacts on the layer of the first dielectric material including a space between adjacent metal contacts;

(d) depositing a layer of a second dielectric material on a top surface of the metal contacts and filling in the space between the metal contacts with the second dielectric material;

(e) removing the second dielectric material from the top surface of the metal contacts and removing an upper portion of the second dielectric material from the filled space between the metal contacts to form a recess;

(f) depositing an additional layer of a first dielectric material on the metal contacts and filling the recess with first dielectric material, wherein the first dielectric material and the second dielectric material have substantially different etch resistance properties;

(g) depositing a layer of a sacrificial metal on the additional layer of the first dielectric material;

(h) depositing a layer of a photoresist on the layer of the sacrificial metal layer;

(k) imagewise removing a portion of the photoresist over some of the metal contacts and optionally over a portion of at least one of the filled recesses adjacent to a side wall of a metal contact;

(l) removing the portion of the layer of the sacrificial metal under the removed portion of the photoresist;

(m) removing the balance of the photoresist layer, and removing the portion of the first dielectric material under the removed portion of the sacrificial metal layer until reaching at least one of the metal contacts and optionally reaching the space filled by the second dielectric material thus forming at least one via through the sacrificial metal layer and through the additional layer of the first dielectric material.

14. The process of claim 13 further comprising:

(n) depositing a layer of a barrier metal on the sacrificial metal layer, and on inside walls and a floor of the at least one via;

(o) filling the at least one via with a fill metal and depositing a layer of a fill metal on the layer of the barrier metal;

(p) removing the fill metal layer, the barrier metal layer and the sacrificial metal layer.

15. The process of claim 13 wherein the first dielectric material is organic and the second dielectric material is inorganic.

16. The process of claim 13 wherein the first dielectric material is inorganic and the second dielectric material is organic.